A Self Calibrating Quadrature Generator with Wide Frequency Range

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Abstract- A quadrature local oscillator generator that produces 0° and 90° amplitude matched signals over a wide frequency range was fabricated using a high performance bipolar technology. This circuit employs a unique phase shifting circuit combined with an improved high frequency phase detector to produce quadrature outputs. RC based circuits, which have typically been used to generate high frequency quadrature signals, can operate only over a narrow frequency range. Other quadrature generation methods such as frequency dividers, use a reference LO frequency at least twice that of the desired quadrature signal and require a duty cycle adjustment circuit which has bandwidth limitations. The circuit described in this paper operates over a frequency range of 400MHz through 700MHz with low amplitude and phase imbalance.

An accurate phase shifter is necessary for communication receivers using an image reject mixer or I/Q downconverter[1][2][3]. The utilization of an image reject mixer eases the requirements of the image filter. Similarly, an I/Q demodulator relies on zero-IF filtering for most of its selectivity, therefore reducing the need for mechanical filters. This circuit utilizes a delay locked loop (DLL) to produce quadrature outputs. The DLL is fully integrated including the loop filter and utilizes a differential architecture. Integration allows the circuit to be self calibrating. The DLL produces quadrature signals which are insensitive to changes in temperature, process, frequency or amplitude.

Fig. 1 depicts the delay locked loop as implemented in the quadrature generator. A Local Oscillator (LO) signal is applied to a single-ended to differential buffer. The output of this buffer drives both the phase shifted and non-shifted paths. The phase shifted path includes a current controlled phase shifter which is followed by a limiting amplifier. The phase shifter delays the incident signal by an amount controlled by a phase detector. The non-phase shifted path includes another limiter matched to the first one. These limiting amplifiers remove gain imbalance introduced by the phase shifter. The outputs of the limiting amplifiers are applied to the phase detector which is based upon an analog multiplier. The phase detector output is filtered and applied to the phase shifter resulting in an output signal phase locked to the reference with a 90° phase offset. The limiting amplifiers also drive output buffers which have been designed for 50Ω matched interfaces.

Stacked architectures are commonly utilized in phase detectors to reduce current consumption. A disadvantage of these circuits is the unequal propagation delays between the inputs. The net effect is a non-zero output when the input signals are at the desired phase difference. This result is detrimental at high frequencies where the inherent propagation delay becomes a significant fraction of the signal time period. The low pass filtered output of an ideal analog multiplier used as a phase detector has a low pass filtered transfer function defined by (1) for inputs $A\cos(\omega t+\alpha)$ and $B\cos(\omega t+\beta)$ where α and β (Fig. 2) represent the phase detector delays. This phase detector will have zero DC output when $\alpha-\beta=90°$.

$$z = \frac{AB}{2}\cos(\alpha-\beta) \quad (1)$$

A similar phase detector which includes propagation delays differing by Δ, has a low pass filtered transfer function defined by (2). This phase detector will have zero DC output when $\alpha-\beta=\Delta+90°$.

$$z = \frac{AB}{2}\cos(\alpha-\beta-\Delta) \quad (2)$$

Fig. 2 depicts a cross-coupling method which uses two phase detectors to reduce the effect of unequal propagation delays. The low pass filtered transfer function of this arrangement is defined by (3). The simulated phase error introduced by the phase detector is improved from 10° to under 0.1° at 500MHz.

$$z = AB\cos(\alpha-\beta)\cos(\Delta) \quad (3)$$

The delay circuit uses two cascaded emitter followers each biased by variable current sources to drive capacitors and provide the appropriate delay. The simplified circuit schematic of a phase shifter is shown in Fig. 3.The phase delay of a single delay stage is defined by (4).

$$\angle\frac{V_o}{V_i} = \operatorname{atan}\left[-\frac{2\pi f C V_T}{I}\right] \quad (4)$$

It can be seen by (4) that if only one emitter follower stage was used, a bias current of zero would be required to achieve the 90° phase shift. This constraint necessitated the use of at least one additional phase shifter.

The quadrature generator was evaluated in an SO-8 package mounted on an FR4 PC board using microstrip lines for all high frequency connections.

Fig. 4 shows the measured phase and amplitude error versus frequency for the quadrature generator. Phase error is defined as the deviation from the expected 90° separation and amplitude error is defined as the difference in the output powers. Less than 1° of phase error was achieved over the frequency range of 435MHz to 660MHz.

Phase noise contribution of the quadrature generator is minimal. Fig. 5 shows the phase noise of the quadrature generator's input source and the phase noise of each of the quadrature generator's outputs. This result shows that the DLL does not degrade the phase noise of either signal.

Greater than 40dB of isolation was measured between the input signal and the outputs as well as between the two quadrature outputs. The actual phase separation of the quadrature outputs will be the vector sum of the intended signal plus the coupled signals. For instance, the coupling of a

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90° phase shifted signal with a 0° phase shifted signal, 40dB lower in amplitude, results in a vector of 89.4° and negligible amplitude change. Lower phase error can be expected when the quadrature generator drives mixers located on the same die rather than driving low impedance external loads.

The quadrature generator operates with a 3V power supply and draws 8mA of current. Current drain is increased by another 4mA to accommodate the low impedance buffers which are used only for evaluation purposes to drive test equipment (50Ω loads).

Fig. 6 through Fig. 12 show the detailed schematics of the circuit used to realized this design.

The test IC (Fig. 13) was fabricated with Motorola's MOSAIC^{TM} V high performance silicon bipolar process to validate the design concepts described by this paper.

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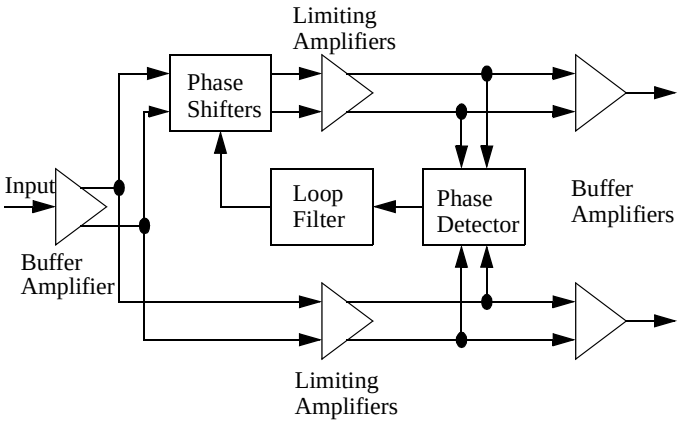

Fig. 1. Quadrature Generator with Delay Locked Loop

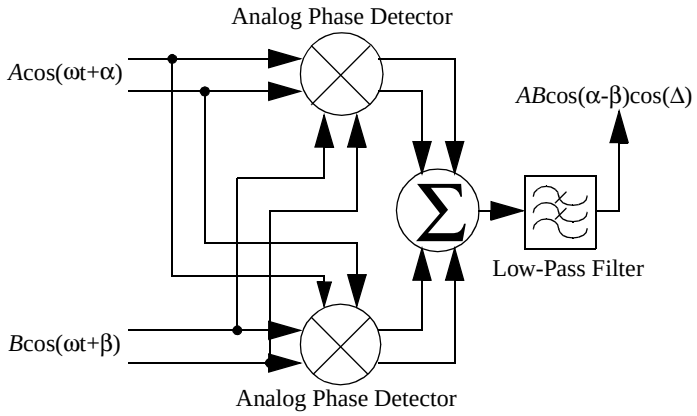

Fig. 2. Phase Detector block diagram

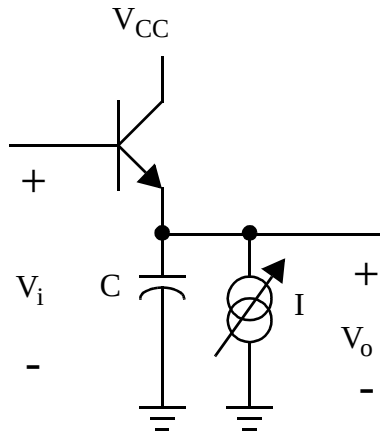

Fig. 3. Phase shifter schematic

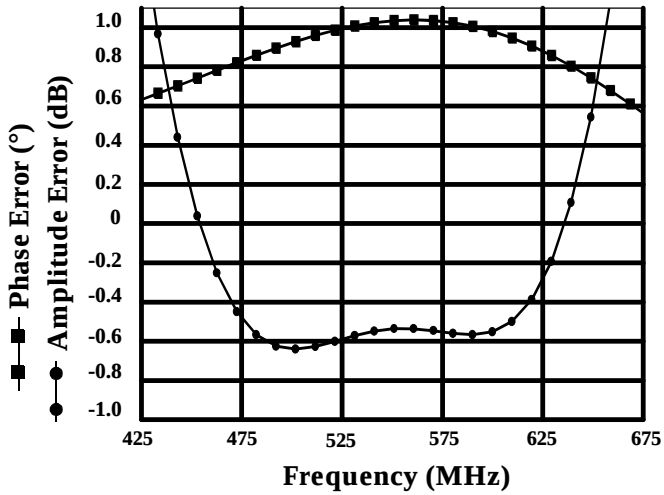

Fig. 4. Amplitude and phase error versus frequency

***References*:**

[1] Jan Crois and Michael Steyaert, "A Fully Integrated 900MHz CMOS Double Quadrature Downconverter," ISSCC Digest of Technical Papers, pp. 136-137, Feb. 1995.

[2] Asad A. Abidi, "Direct-Conversion Radio Transceivers for Digital Communications," IEEE Journal of Solid-State Circuits, Vol. 30, No. 12, pp. 1399-1410, Dec. 1995.

[3] Shoji Otaka, et. al., "A Low Local Input 1.9GHz Si-Bipolar Quadrature Modulator with No Adjustment," IEEE Journal of Solid-State Circuits, Vol. 31, No. 1, Jan. 1996

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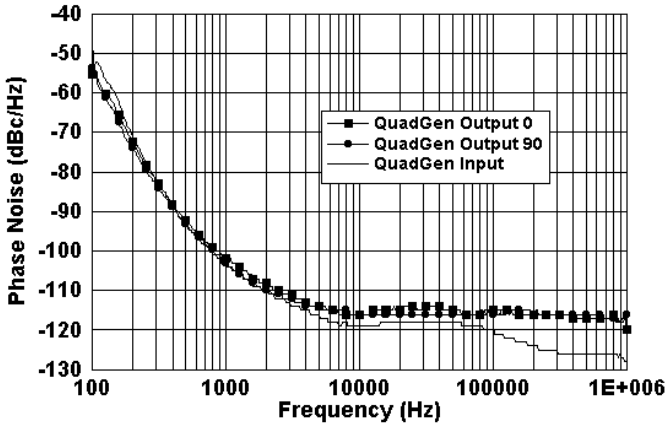

Fig. 5. Phase noise of quadrature input and each output

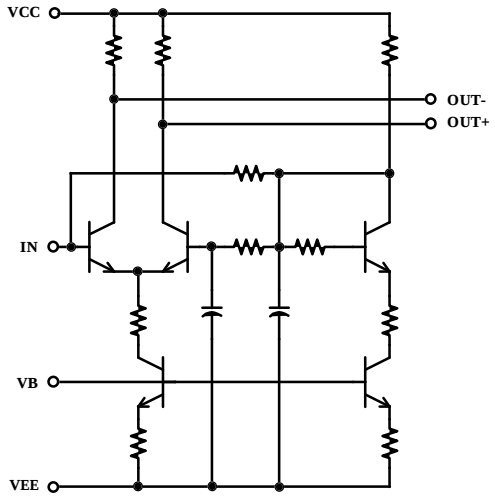

Fig. 8. Quadrature Generator Single-Ended to Differential Buffer Schematic

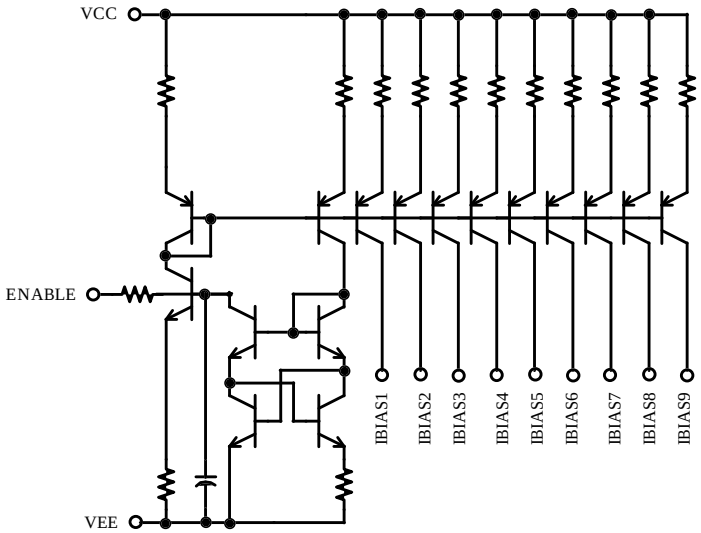

Fig. 6. Quadrature Generator DC Bias Schematic

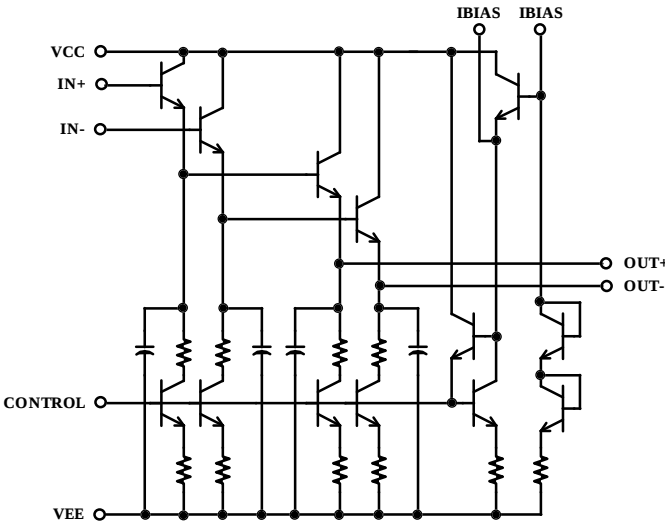

Fig. 9. Quadrature Generator Phase Shifter Schematic

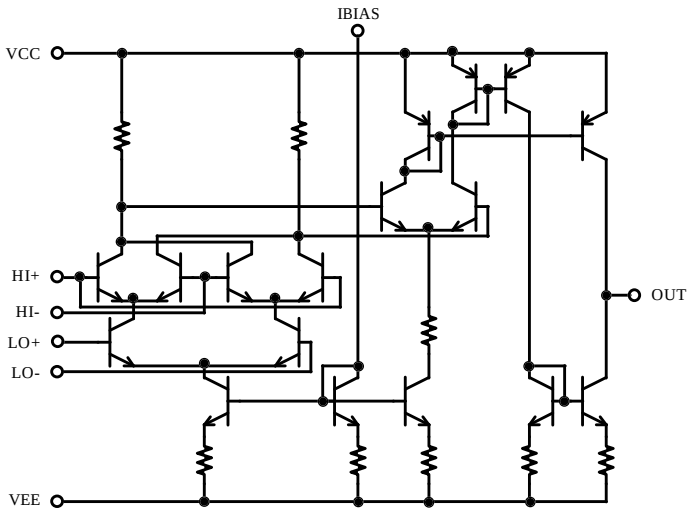

Fig. 7. Quadrature Generator Phase Detector Schematic

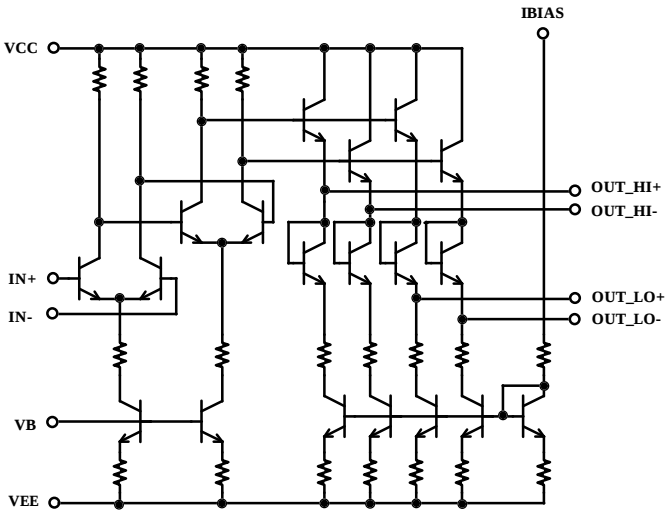

Fig. 10. Quadrature Generator Limiting Amplifier and Buffer Schematic

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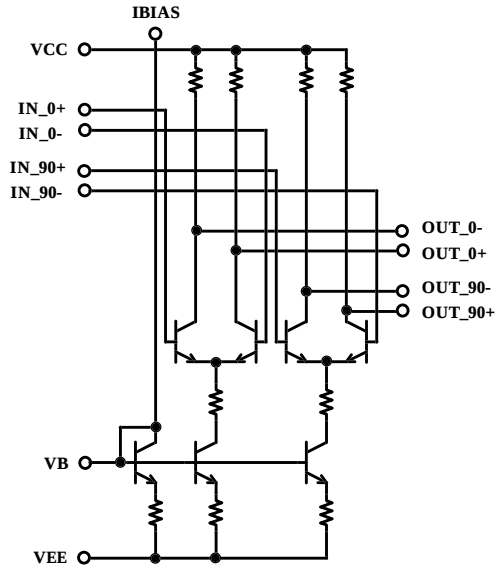

Fig. 11. Quadrature Generator Differential Buffer Schematic

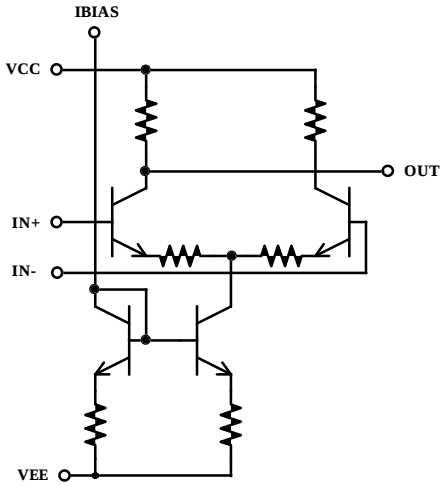

Fig. 12. Quadrature Generator 50Ω Buffer Schematic

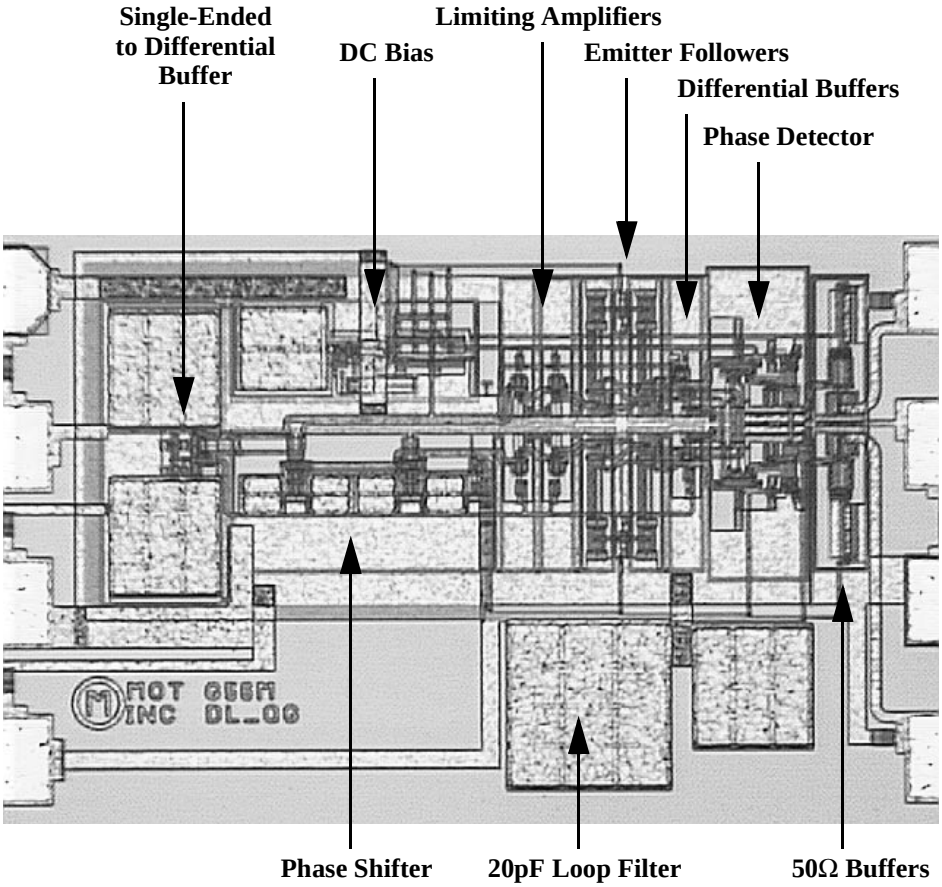

Fig. 13. Photograph of the test IC.